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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/882,076 | 06/15/2001 | Stephane G. Plante | 50037.08US01 | 8789 |

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| EXAMINER | |
|---|---|
| SURYAWANSHI, SURESH | |
| **ART UNIT** | **PAPER NUMBER** |
| 2115 | |

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/882,076 | PLANTE ET AL. | |
| | Examiner | Art Unit | |
| | Suresh K. Suryawanshi | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *7/21/05 declaration under 37 CFR 1.131*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-23 are presented for examination.

### *Claim Rejections - 35 USC § 101*

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 11-17 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

4. Claims 11-17 are not limited to tangible embodiments. In view of applicant's disclosure, specification page 4, line 18 -- page 5, line 14, the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., magnetic disk storage) and intangible embodiments (e.g., carrier wave). As such, the claims are not limited to statutory subject matter and are therefore non-statutory.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7, 10-11, 14-19 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kung et al (US Patent No. 6,574,739 B1; hereinafter Kung) in view of Fruehling et al (US Patent No. 6,625,688 B1[1]; hereinafter Fruehling).

7. As per claim 1, Kung discloses

measuring a prior utilization of the computer [Fig. 1; col. 2, lines 47-55; col. 3, lines 46-50; col. 6, lines 44-48; CPU activity monitoring circuit]; and

if the prior utilization crosses a threshold, modifying a parameter associated with the CPU [Fig. 2; col. 1, lines 48-51, 57-67; col. 2, lines 47-57; col. 46-50; col. 4, line 22 -- col. 5, line 25; col. 6, lines 49-52; col. 7, lines 13-17; changing the input voltage of the CPU or changing the internal clock frequency of the CPU when the perceived load of the CPU crosses at least a predetermined threshold value].

[1] Prior art cited by the examiner in the prior office action.

Kung does not expressly disclose about determining the utilization of the CPU while the CPU is idle. But, Kung discloses that the utilization request could be periodic or may be in response to a signal [col. 4, lines 43-45; a timer to interrupt; col. 4, lines 9-10; based upon the M/IO signal line]. However, Fruehling clearly discloses about a CPU performing a comparison task during an idle cycle of the CPU [Fig. 6B, 6D, 7A; detect CPU_idle_Bus; col. 18, lines 4-7, 43, 50; col. 20, lines 1-8; col. 11, lines 32-34; col. 12, lines 60-63; col. 13, lines 46-47]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the CPU idle cycle (i.e., while there is no load) to determine the CPU utilization. Moreover, it would clearly be a time efficient to utilize the idle cycle of the CPU to determine the utilization of the CPU and throttle it accordingly.

8. As per claim 11, Kung discloses

calculating a prior utilization of the CPU [Fig. 1; col. 2, lines 47-55; col. 3, lines 46-50; col. 6, lines 44-48; CPU activity monitoring circuit]; and

calculating a utilizable CPU performance level sing the prior utilization [Fig. 2; col. 1, lines 48-51, 57-67; col. 2, lines 47-57; col. 46-50; col. 4, line 22 -- col. 5, line 25; col. 6, lines 49-52; col. 7, lines 13-17; changing the input voltage of the CPU or changing the internal clock frequency of the CPU when the perceived load of the CPU crosses at least a predetermined threshold value].

Kung does not expressly disclose about determining the utilization of the CPU while the CPU is idle. But, Kung discloses that the utilization request could be periodic or may be in response to a signal [col. 4, lines 43-45; a timer to interrupt; col. 4, lines 9-10; based upon the M/IO signal line]. However, Fruehling clearly discloses about a CPU performing a comparison task during an idle cycle of the CPU [Fig. 6B, 6D, 7A; detect CPU_idle_Bus; col. 18, lines 4-7, 43, 50; col. 20, lines 1-8; col. 11, lines 32-34; col. 12, lines 60-63; col. 13, lines 46-47]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the CPU idle cycle (i.e., while there is no load) to determine the CPU utilization. Moreover, it would clearly be a time efficient to utilize the idle cycle of the CPU to determine the utilization of the CPU and throttle it accordingly.

9. As per claim 18, Kung discloses

a CPU utilization monitor configured to monitor a utilization of the CPU [Fig. 1; col. 2, lines 47-55; col. 3, lines 46-50; col. 6, lines 44-48; CPU activity monitoring circuit];

a CPU throttler configured to perform the adaptive throttling of the CPU based on information from the CPU utilization monitor [Fig. 2; col. 1, lines 48-51, 57-67; col. 2, lines 47-57; col. 46-50; col. 4, line 22 -- col. 5, line 25; col. 6, lines 49-52; col. 7, lines 13-17; changing the internal clock frequency of the CPU when the perceived load of the CPU crosses at least a predetermined threshold value]; and

a timer configured to monitor a time since an idle state [col. 3, lines 40-50; col. 4, lines 43-47; col. 5, line 62 -- col. 6, line 4; a timer].

Kung does not expressly disclose about determining the utilization of the CPU and activating the CPU throttler while the CPU is idle. But, Kung discloses that the utilization request could be periodic or may be in response to a signal [col. 4, lines 43-45; a timer to interrupt; col. 4, lines 9-10; based upon the M/IO signal line]. However, Fruehling clearly discloses about a CPU performing a comparison task during an idle cycle of the CPU [Fig. 6B, 6D, 7A; detect CPU_idle_Bus; col. 18, lines 4-7, 43, 50; col. 20, lines 1-8; col. 11, lines 32-34; col. 12, lines 60-63; col. 13, lines 46-47]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the CPU idle cycle (i.e., while there is no load) to determine the CPU utilization. Moreover, it would clearly be a time efficient to utilize the idle cycle of the CPU to determine the utilization of the CPU and throttle it accordingly.

10. As per claim 2, Kung discloses that the parameter comprises a clock frequency [col. 6, lines 49-52; internal clock frequency].

11. As per claim 3, Kung discloses that the parameter comprises a voltage [col. 6, lines 49-52; input voltage].

12. As per claim 4, Kung discloses storing the prior utilization in a utilization history database [col. 6, lines 17-24; inherent to the system as it matches the processor speed and the voltage with the perceived processing load].

13. As per claim 5, Kung discloses accessing the utilization history database to determine if the CPU has been at a performance level for a sufficient period of time [col. 3, lines 40-46; col. 5, line 62 -- col. 6, line 4; col. 6, lines 17-24; inherent to the system as the timer will indicate the period of time the CPU stayed in a state indicated by M/IO signal].

14. As per claim 6, Kung discloses that the threshold indicates that a performance level allocated with the CPU should be increased [Fig. 2].

15. As per claim 7, Kung discloses applying a system policy to determine whether to increase the performance level of the CPU [Fig. 2].

16. As per claim 10, Kung and Fruehling disclose the invention substantially. Kung and Fruehling do not expressly disclose about a switching latency of the CPU. However, a routineer in the art would know about a switching latency of a CPU and typically the latency due to performance state transition is limited to no more than approximately two hundred microseconds. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system policy so that it relates to a switching latency of the CPU.

17. As per claim 14, Kung discloses changing the CPU performance level to the utilizable CPU performance level [Fig. 2; col. 1, lines 48-51, 57-67; col. 2, lines 47-57; col. 46-50; col. 4, line 22 -- col. 5, line 25; col. 6, lines 49-52; col. 7, lines 13-17; changing the input voltage of the CPU or changing the internal clock frequency of the CPU when the perceived load of the CPU crosses at least a predetermined threshold value].

18. As per claim 15, Kung discloses changing the CPU performance level occurs at an expiration of a timer [col. 3, lines 40-50; col. 4, lines 43-47; col. 5, line 62 -- col. 6, line 4; a timer].

19. As per claim 16, Kung discloses if the minimum performance level is equal to a maximum performance level of the CPU, disabling the timer [inherent to the system as there is no more performance level to change].

20. As per claim 17, Kung discloses if the new performance level is less than a maximum performance level of the CPU, resetting the time [inherent to the system as there is more than one performance level to change].

21. As per claim 19, Kung discloses that the CPU is activated when the time since the last idle state exceeds a threshold [col. 3, lines 40-50; col. 4, lines 43-47; col. 5, line 62 -- col. 6, line 4; a timer].

22. As per claim 22, Kung discloses that the CPU throttler changes the CPU performance level in response a utilization of the CPU measured by the CPU utilization monitor [Fig. 2; col. 1, lines 48-51, 57-67; col. 2, lines 47-57; col. 46-50; col. 4, line 22 -- col. 5, line 25; col. 6, lines 49-52; col. 7, lines 13-17; changing the internal clock frequency of the CPU when the perceived load of the CPU crosses at least a predetermined threshold value].

23. As per claim 23, Kung discloses that upon activation, the CPU throttler resets the timer [inherent to the system as to initialize the timer for next time].

24. Claims 8-9, 12-13 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kung et al (US Patent No. 6,574,739 B1; hereinafter Kung), Fruehling et al (US Patent No. 6,625,688 B1[1]; hereinafter Fruehling) and in view of Mittal et al (US Patent No. 5,719,800; hereinafter Mittal).

25. As per claims 8, 12 and 20, Kung and Fruehling disclose the invention substantially. Kung and Fruehling do not expressly disclose about a performance limit related to the temperature. However, Mittal expressly discloses that it is well known in the art [col. 1, lines 28-35]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the temperature as a performance limiter in the system policy. Moreover, a routineer would like to keep an eye on the temperature to avoid overheating of the system as the system starts quickly heating up during high performance level.

26. As per claims 9, 13 and 21, Kung and Fruehling disclose the invention substantially. Kung and Fruehling do not expressly disclose about a performance limit related to a battery level. However, Mittal expressly discloses that it is well known in the art [col. 1, lines 52-67]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the battery level as a performance limiter in the system policy. Moreover, a routineer would like to keep an eye on the battery level to avoid a sudden power down of the system as the system starts quickly loosing battery power during high performance level.

***Response to Arguments***

27. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
August 1, 2005